

REMARKS

Claims 1-8 are pending in the Application.

Claims 1-8 stand rejected.

I. OBJECTION TO THE DRAWINGS

The drawings have been objected to as failing to comply with 37 C.F.R. §1.84(p)(5) because they include reference signs not mentioned in the Description. The Applicants have filed concurrently herewith corrected drawings deleting reference signs not mentioned in the Description. Also, as noted hereinabove, formal drawings have been filed to replace the informal drawings previously submitted.

Additionally, Figures 1.2(C) and 1.4 were objected to as failing to include a legend such as "Prior Art." New Figures 1.2(C) and 1.4 have been filed concurrently herewith bearing the legend "Prior Art."

II. OBJECTION TO THE SPECIFICATION

The Abstract has been objected to because of the trailer. A new Abstract is filed concurrently herewith having the trailer removed.

The written description has been objected to because of the informality in the cross-references to the related applications. The cross-reference to the related applications has been amended hereinabove to include the serial numbers of the applications therein.

Additionally, the Specification has been objected to in that the equation on page 3, line 11 is missing a right parenthesis. The Applicants have amended the paragraph beginning at line 9 on page 3 to correct the missing right parenthesis. Additionally, the equation appearing therein has been rewritten to replace the exponent, -1 appearing

therein with $-i$ which conforms the expression with Figure 1.2C. Likewise, the index has been corrected to run from 0 to n .

The Examiner has also asserted that Drawings 1.2A, 1.2B, 1.3 and 1.5X have not been mentioned in the Specification. The Applicants note that there is no Drawing 1.5X. The Applicants understand that the reference to Figure 1.5X should be 1.5A. The Applicants also note that Figure 1.2A is referred to on page 6 at line 23. Likewise, Figure 1.2B is referred to on page 6 at line 28 and on page 7 at line 10. Figure 1.3 is referred to on page 7, at line 13. Figure 1.5A is discussed on page 8 at line 17.

In view of the foregoing, the Applicants respectfully request the withdrawal of the objections to the Specification.

III. REJECTION UNDER 35 U.S.C. §112, FIRST PARAGRAPH

Claims 1-8 have been rejected under 35 U.S.C. §112, first paragraph as containing subject matter which was not described in the Specification in such a way as to enable one skilled in the art to which it pertains, or with which it is most nearly connected to make and use the invention. The Applicants respectfully traverse the rejection of claims 1-8 under 35 U.S.C. §112, first paragraph.

The Examiner contends that the Specification briefly mentions the output mechanisms selectively providing either the fully settled data or all data from the FIR filter. (Paper No. 7, page 3.) The Examiner also states that the Specification does not clearly explain in full detail how the integrated circuit is structured and operated to provide a control mechanism for selectively providing the desired data from the FIR filter.

The Examiner's requirement that the Specification explain in full detail how the integrated circuit is structured and operated . . . is not the test for enablement. The

standard for determining whether a Specification meets the enablement requirement is whether undue experimentation is needed to practice the invention. M.P.E.P. §2164.01. The Examiner must show how one reasonably skilled in the art would be unable, without undue experimentation, to make or use the invention in view of the disclosures in the Application coupled with information known in the art. *Id.* This, the Examiner has not done.

Moreover, the Applicants explain that in the operation of a FIR filter, during filling of the delay pipeline, the output gives a result that holds information about the input but does not present the data with the same scaling and frequency content as the fully settled filter. (Description of the Preferred Embodiment, page 7, lines 1-4.) (That the output is the sum of taps is described in the Description of the Preferred Embodiment, page 3, lines 9-13.) Thus, as the Applicants teach, a settle mode may be selected by applying a voltage to a pin, or, alternatively, by setting a mode bit. (Description of the Preferred Embodiment, page 7, lines 10-12.) The inhibition of the output of a serial port in response to such a select voltage would be within the skill of persons of ordinary skill in the art. For example, it is understood in the art that an output port may be inhibited by "tristating" the port. (Tristating would be recognized by those of ordinary skill in the art as referring to setting the pin to a high impedance state. Other schemes could also be used, such as setting the pin to a predetermined logic level. It would be appreciated by those of ordinary skill in the art that device data sheets commonly specify the initial condition of the I/O pins to permit the user to interface external circuitry to the device.) The Applicants also point out that the pipeline fills at the n th sample of the input. (Description of the Preferred Embodiment, page 7, line 1.) Thus, it would be appreciated by one of ordinary skill in the art that the output may be asserted by counting n filter clock cycles elapsed after the reset operation. Thus, the Applicants respectfully submit that the Disclosure discusses more than a brief mention of an output mechanism selectively providing either fully settled data or unsettled data. Additionally,

the Applicants also respectfully contend that one of ordinary skill in the art, in view of the foregoing, would be able to make and use the invention without undue experimentation. Consequently, the Applicants respectfully request the rejection of claims 1-8 under 35 U.S.C. §112, first paragraph be withdrawn.

IV. REJECTION UNDER 35 U.S.C. §112, SECOND PARAGRAPH

Claims 1-8 have been rejected under 35 U.S.C. §112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which the Applicants regard as the invention. The Applicants respectfully traverse the rejection of claims 1-8 under 35 U.S.C. §112, second paragraph.

The Examiner contends that claim 1, for example, is indefinite in so far as what the limitations “fully settled data” and “all data” mean. The Applicants respectfully disagree that this raises a ground of rejection under 35 U.S.C. §112, second paragraph. The essential inquiry in determining whether the claim language satisfies the requirements under 35 U.S.C. §112, second paragraph is whether the claims set out and circumscribe a particular subject matter with a reasonable degree of clarity and particularity. M.P.E.P. §2173.02. In particular, the definiteness of claim language is analyzed not in vacuum but in the light of, *inter alia*, the application disclosure. *Id.* As discussed hereinabove, the Applicants describe the characteristics of a FIR filter and the settling of the output data thereof. Additionally, claim 1 itself expressly states “all data from the FIR filter, including unsettled data.” The Applicants respectfully submit that in view of the Specification, including the claim language itself, that a person of ordinary skill in the art would know whether his or her particular device output data from a FIR filter only after the data settled, or output all the data, that is, including unsettled data. The Examiner has raised no assertion to the contrary. Therefore, the Applicants respectfully contend that the language of claim 1 (and claims depending therefrom)

informs the public as to the scope of the claims, that is, the boundaries of what constitutes infringement of the patent, and therefore, satisfy the requirements of 35 U.S.C. §112, second paragraph. See M.P.E.P. §2173.

In view of the foregoing, the Applicants respectfully request the Examiner to withdraw the rejections of claims 1-8 under 35 U.S.C. §112, second paragraph.

V. REJECTION UNDER 35 U.S.C. § 103

Claims 1-8 have been rejected under 35 U.S.C. §103 as being obvious over *Cabler et al.*, U.S. Patent No. 5,656,621 ("the *Cabler* reference"). The Applicants respectfully traverse the rejection of claims 1-8 under 35 U.S.C. §103.

Claim 1 is directed to an integrated circuit. The integrated circuit of claim 1 includes an analog-to-digital converter, a FIR filter, and an output mechanism providing either only fully settled data from the FIR filter or all data from the FIR filter, including unsettled data. The Examiner asserts that *Cabler* discloses an integrated circuit including an analog-to-digital converter and a FIR filter. The Examiner admits that *Cabler* does not disclose an output mechanism selectively providing either only fully settled data from the FIR filter or all data from the FIR filter. (Paper No. 7, page 4.) However, the Examiner asserts that *Cabler* discloses, in Figure 2, an output mechanism (reference 602) selectively providing either a partial result or a full result from the FIR filter (reference 677) using a control signal (reference 604). The Applicants respectfully disagree. In fact, *Cabler* teaches that the output mechanism identified by the Examiner is a record multiplexer (602). (The *Cabler* reference, Figure 2, and column 19, lines 13-14.) The record multiplexer selects analog audio signals in response to the status of control register CLICI (604). (*Id.*) Note that mux 602 is part of mixer 606. (The *Cabler* reference, Figure 2 and column 19, lines 11-13.) The *Cabler* reference further teaches

that mixer **606** is part of Mixing and Analog Functions Block **510**. (The *Cabler* reference, column 6, lines 5-6.) Note that the output of Mixing and Analog Functions Block **510** feeds the input of ADC block **516**. (The *Cabler* reference, Figure 1.) Thus, multiplexer **602** provides an analog signal to an ADC. (See *also* the *Cabler* reference, Figure 2) (showing the output of multiplexer **602** input to left record ADC **666**.) Furthermore, reference **677** is not the output of a FIR filter. Reference **677** is the main mixer loop-back path that provides the output of the main mixer (**698**) to the input of mux **602**. (The *Cabler* reference, column 19, lines 37-38.) (Main mixer **698** is an analog mixer; it outputs an analog signal that is the sum of a plurality of input analog signals. The *Cabler* reference, column 19, lines 18-19.) The loop-back path is for system test and dub-over capability (See *Cabler* reference, column 19, lines 21-22.)

Thus, the teaching relied upon by the Examiner does not disclose an output mechanism selectively providing either a partial result or a full result from a FIR filter, as the Examiner contends.

The Examiner also asserts that it would have been obvious to one of ordinary skill in the art to add an output mechanism selector into Figure 2 of the *Cabler* reference for selecting the desired results to the FIR filter of Figure 1 because it would enable the operator to select the desired signals, to reduce the initial unsteady state and to increase the immunity from process variation. However, as noted above, the *Cabler* reference has not been shown to teach either an output mechanism for selectively providing a full or partial result from the FIR filter. Moreover, the asserted motivation to modify the teachings of *Cabler* do not address the limitations of claim 1. Claim 1 does not recite mechanisms for selecting desired results to a FIR filter. Moreover, the alleged motivation of selecting desired signals to reduce the initial unsteady state, etc., are not found in one of the three sources of such a motivation. (See M.P.E.P. §2143.01.)

Furthermore, these are not clear and particular statements of a motivation or suggestion to combine references, but broad conclusory statements regarding the teachings of the reference itself. Such broad conclusory statements are not evidence. *In re Lee*, 277 F.3d 1338, 1343, 61 U.S.P.Q.2d 1430, 1433-34 (Fed. Cir. 2002); *In re Kotzab*, 217 F.3d 1365, 1370, 55 U.S.P.Q.2d 1313, 1317 (Fed. Cir. 2000); *In re Dembiczak*, 175 F.3d 994, 999, 50 U.S.P.Q.2d 1614, 1616 (Fed. Cir. 1999).

Therefore, for at least the aforesaid reasons, the Applicants respectfully assert that a *prima facie* showing of obviousness has not been made with respect to claim 1. Consequently, claim 1 is allowable under 35 U.S.C. §103 over the *Cabler* reference. M.P.E.P. §2143.

Claim 2 is directed to the integrated circuit of claim 1 in which the output mechanism includes an external pin on the integrated circuit to which a user can apply a control signal to control the selection of fully settled data from the FIR filter or all the data from the FIR filter, including unsettled data. The Examiner asserts that the *Cabler* reference teaches the limitation of claim 2 in disclosing CLICI 604 in Figure 2. (Paper No. 7, page 5.) However, as previously discussed hereinabove, signal CLICI 604 controls an analog mux. (The *Cabler* reference, column 19, lines 12-13.) CLICI 604 has nothing to do with controlling the selection of data from a FIR filter.

Therefore, for at least the aforesaid reasons, the *Cabler* reference has not been shown to teach or suggest all of the limitations of claim 2. Neither has a motivation upon which a *prima facie* showing of obviousness been provided. Therefore, the Applicants respectfully contend that claim 2 is allowable over the *Cabler* reference.

Claim 3 is directed to the integrated circuit of claim 1 in which the output mechanism comprises one or more bits on a register of the integrated circuit to which a user can set to control the selection of fully settled data from the FIR filter or all data from the FIR filter, including unsettled data. The Examiner contends that the limitation of claim 3 is disclosed in *Cabler* in teaching registers 566, Figure 7. (Paper No. 7, page 5.) However, registers 566 are not registers to which a user can set to control the selection of fully settled data from a FIR filter. Registers 566 are explicitly disclosed in the *Cabler* reference to control the respective attenuations/gain control circuits and the attenuation/gain range for the circuits for each of the analog gain blocks in Figure 2. (The *Cabler* reference, column 6, lines 23-28.) Thus, the Examiner has not shown that the *Cabler* references teaches or suggests all of the limitations of claim 3. Neither has a motivation or suggestion for modifying the *Cabler* reference to make the invention of claim 3 been provided. Therefore, the Applicants respectfully contend that a *prima facie* showing of obviousness has not been made with respect to claim 3, and claim 3 is allowable over the *Cabler* reference.

Claim 4 further depends from claim 3 and recites the integrated circuit thereof in which the one or more bits on a register of the integrated circuit are set over a serial port interface. The Examiner contends that the limitation of claim 4 is taught by *Cabler* in disclosing serial EEPROM 570. As an initial matter, the Applicants note that a serial EEPROM is not a serial port. A serial EEPROM is a memory device. Additionally, the *Cabler* reference teaches that serial EEPROM 570 is used by the CODEC to make the CODEC Plug-and-Play compatible with industry standard buses. (The *Cabler* reference, column 36, lines 10-13.) Serial EEPROM 570 is external to the circuitry taught in the *Cabler* reference and operates in conjunction with external CD-ROM interface 568. (The *Cabler* reference, column 36, lines 13-20.) Thus, the *Cabler* reference has not been shown to teach or suggest all of the limitations of claim 4.

Neither has a motivation or suggestion for modifying the *Cabler* reference to make the invention of claim 4 been provided. Therefore, the Applicants respectfully assert that a *prima facie* showing of obviousness has not been made with respect to claim 4, and claim 4 is therefore allowable under 35 U.S.C. §103 over the *Cabler* reference.

Claim 5 is directed to the integrated circuit of claim 1 in which the analog-to-digital converter is a delta-sigma modulator. Although the Applicants do not dispute that the *Cabler* reference teaches a delta-sigma modulator ADC, claim 5 is not directed to a delta sigma modulator ADC standing alone. For the reasons discussed hereinabove, the *Cabler* reference has not been shown to teach a delta-sigma ADC in an integrated circuit including the ADC, a FIR filter and an output mechanism selectively providing either only fully settled data from the FIR or all the data from the FIR including unsettled data. Therefore, the *Cabler* reference has not been shown to teach or suggest all of the limitations of claim 5. Neither has a motivation or suggestion for modifying the *Cabler* reference to make the invention of claim 5 been provided. Thus, the Applicants respectfully assert that a *prima facie* showing of obviousness has not been made with respect to claim 5, and claim 5 is allowable under 35 U.S.C. §103 over the *Cabler* reference.

Claim 6 depends from claim 1 and recites the integrated circuit thereof in which the FIR filter is a decimation filter. Again, the Applicants do not dispute that *Cabler* teaches a FIR decimation filter. However, again, the *Cabler* reference has not been shown to teach or suggest a FIR decimation filter as recited in claim 6, which includes the limitations of claim 1 from which it depends. Consequently, for at least these reasons, a *prima facie* showing of obviousness has not been made with respect to claim 6, and claim 6 is allowable over the *Cabler* reference.

Claim 7 is directed to a method of designing an integrated circuit having a FIR filter. The method includes the step of providing a mechanism to permit a user to select either only fully settled data from the FIR filter or all data from the FIR filter, including unsettled data. Claim 7 has been rejected on the same rationale as claim 1. (Paper No. 7, page 5.) For at least the reasons discussed hereinabove in conjunction with claim 1, the Applicants respectfully contend that the *Cabler* reference has not been shown to teach or suggest a method of designing an integrated circuit having a FIR filter including a step of providing a mechanism to permit the user to select either or only fully settled data from the FIR filter or all data from the FIR filter. As previously discussed, the Examiner has identified no teaching in the *Cabler* reference whatsoever directed to selecting data from a FIR filter. Thus, because, for at least the reasons that the *Cabler* has not been shown to teach or suggest all of the limitations of claim 7, nor has there been provided a motivation or suggestion for modifying the *Cabler* reference to make the invention of claim 7 sufficient to sustain a *prima facie* showing of obviousness, the Applicants respectfully assert that claim 7 is allowable under 35 U.S.C. §103 over the *Cabler* reference.

Claim 8 is directed to a method of fabricating an integrated circuit having a FIR filter, the method includes the step of providing a mechanism to permit a user to select either only fully settled data from the FIR filter or all data from the FIR filter. Claim 8 has also been rejected on the same rationale as claim 1. (Paper No. 7, page 5.) The Applicants also respectfully contend that claim 8 is allowable under 35 U.S.C. §103 over the *Cabler* reference for at least the reasons that the *Cabler* reference has not been shown to teach or suggest a mechanism permitting a user to select either fully settled data or all the data from the FIR filter, as previously discussed.

VI. CONCLUSION

As a result of the foregoing, it is asserted by Applicants that the claims as respectively amended or added in the Application, are in condition for allowance, and Applicants respectfully request an early allowance of such claims.

Applicants respectfully request that the Examiner call Applicants' attorney at the below listed number if the Examiner believes that such a discussion would be helpful in resolving any remaining problems.

Respectfully submitted,

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Serial No. 09/695,704
 Amendment Dated Aug 15, 2003
 Annotated Sheet Showing Changes

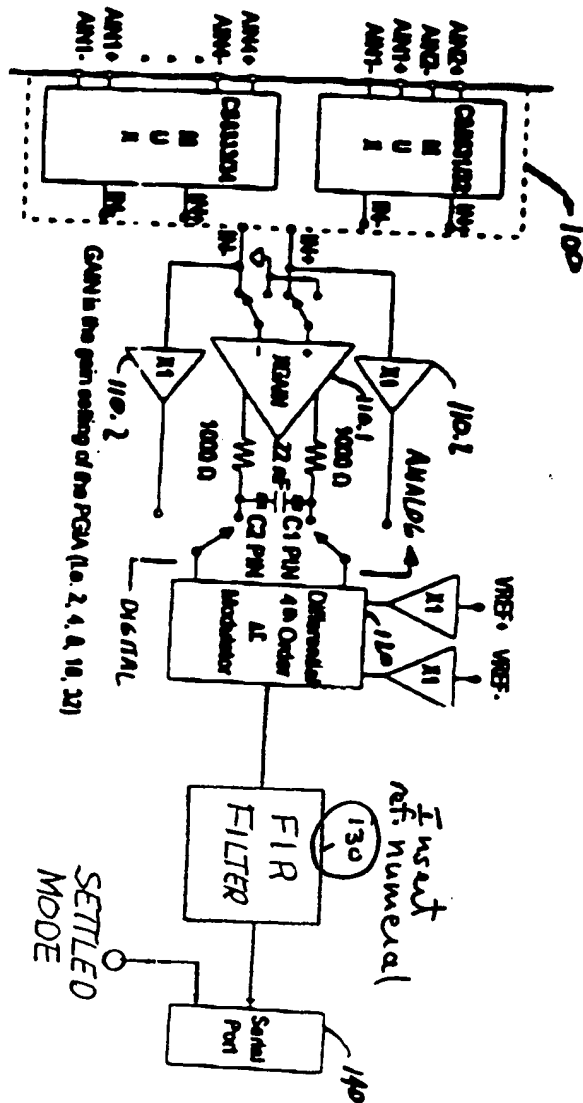


FIGURE 1.2 B

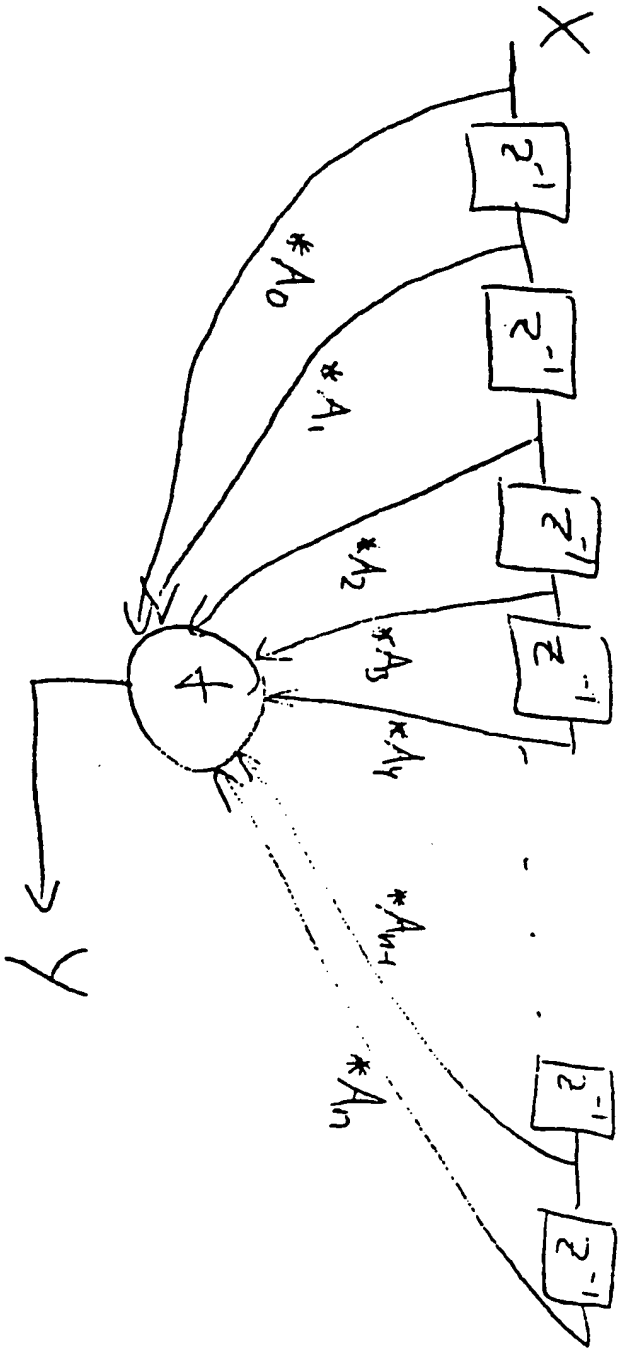


FIG 1.2c
(Prior Art)
Insert

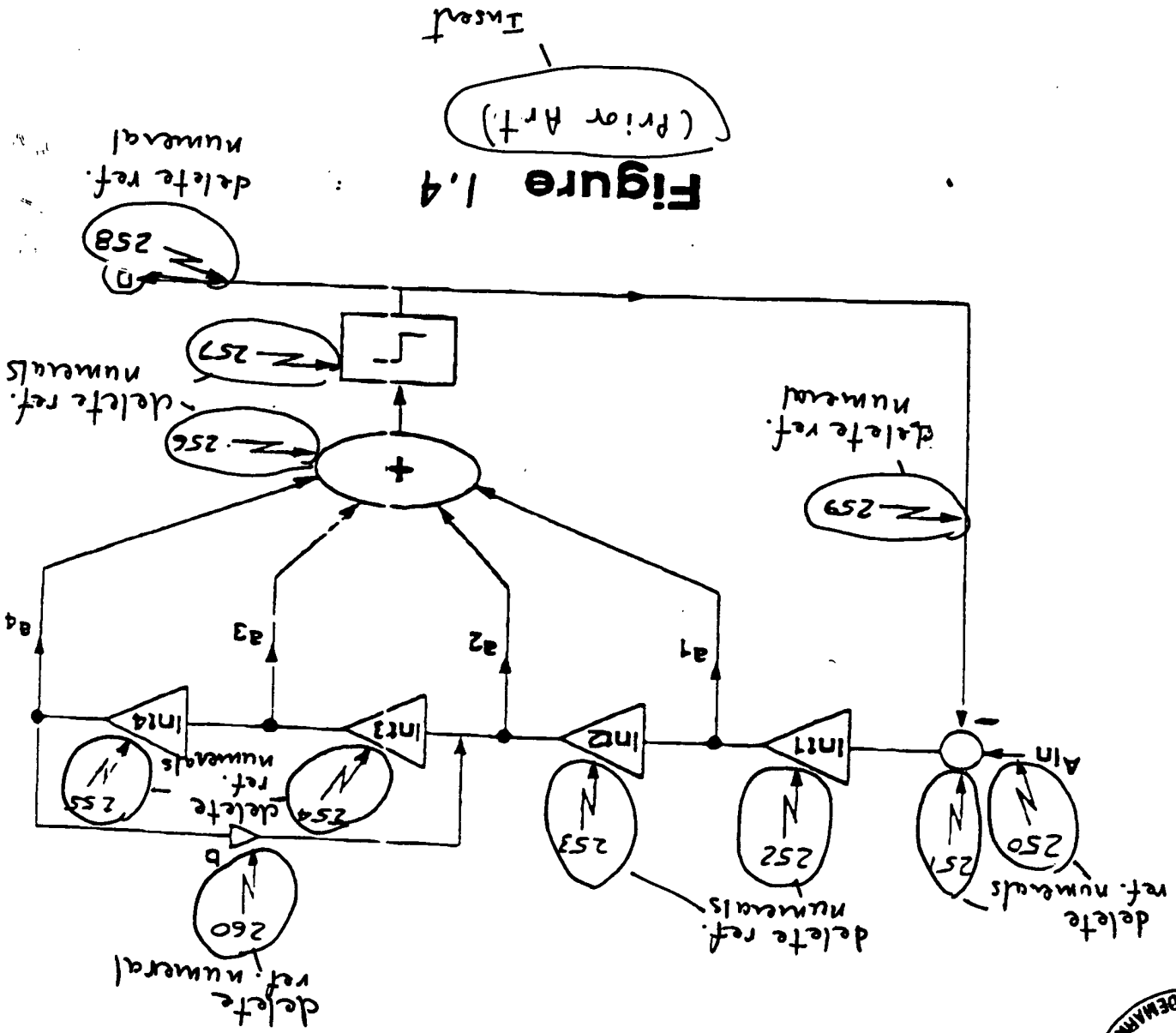


Figure 1,4
 (Prior Art)
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delete title

DIGITAL BLOCK DIAGRAM

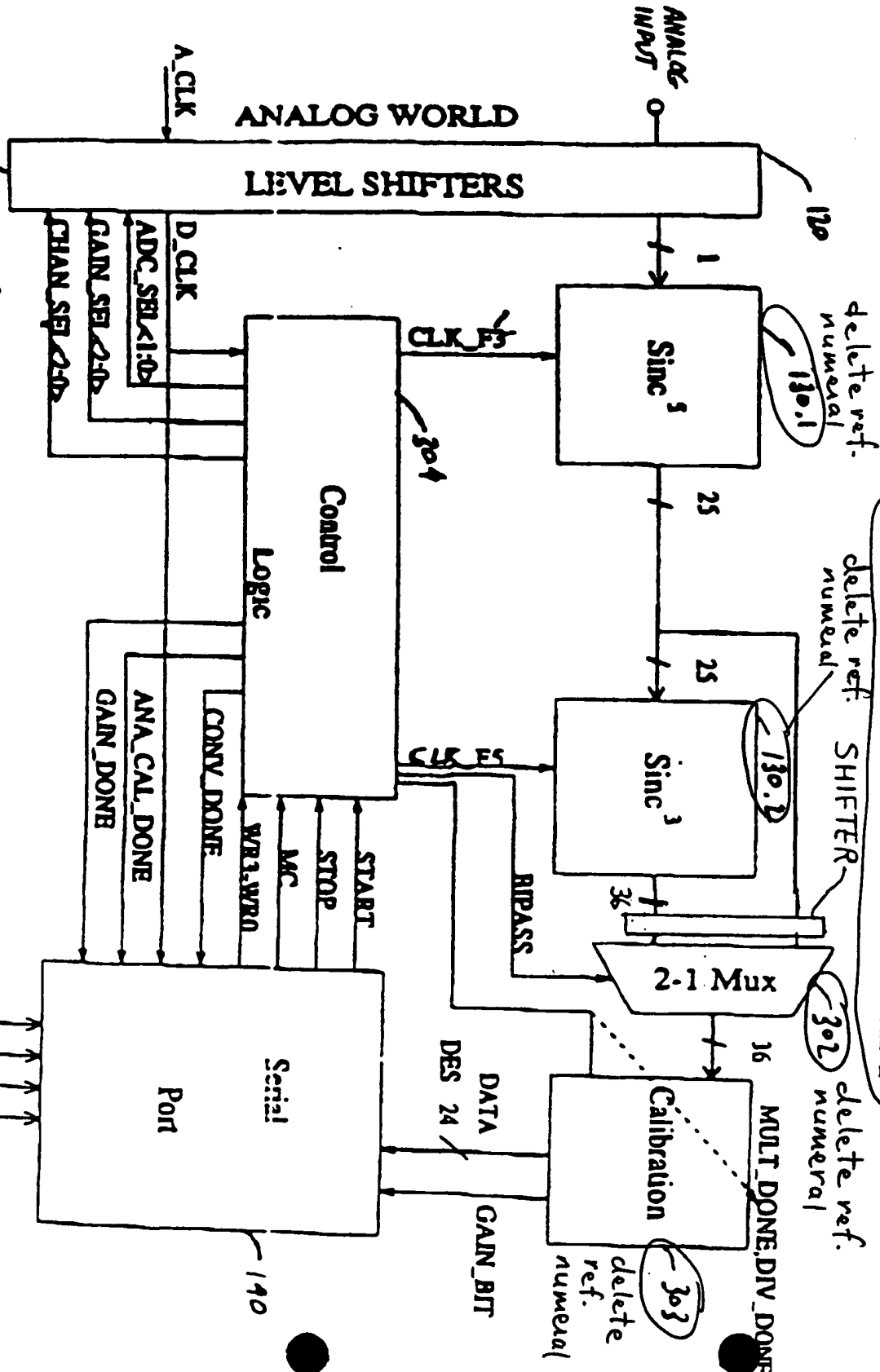


Fig. 2.3

Figure 1.5A

DIGITAL BLOCK DIAGRAM

delete title

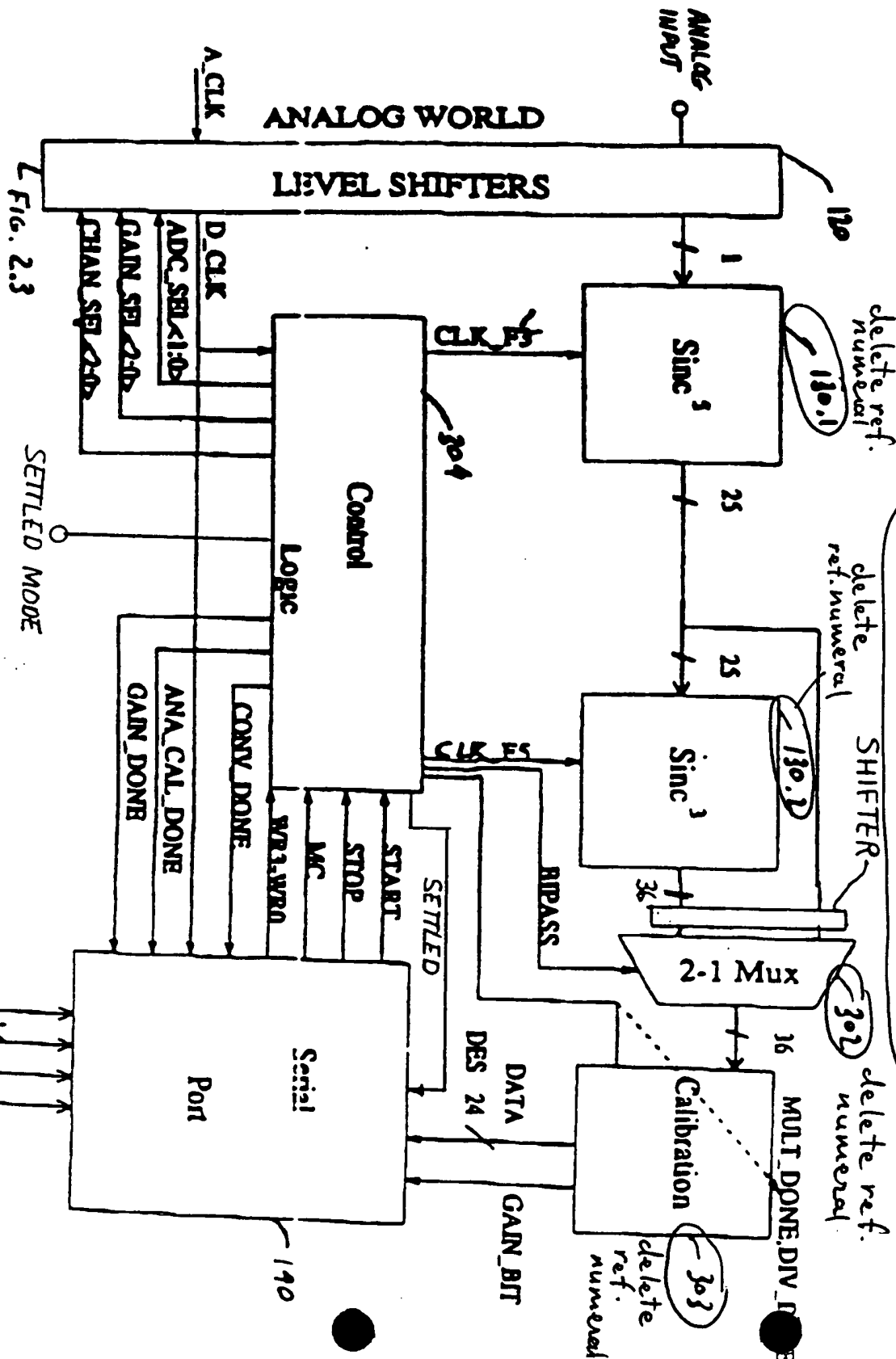


Fig. 2.3

Figure 1.5R

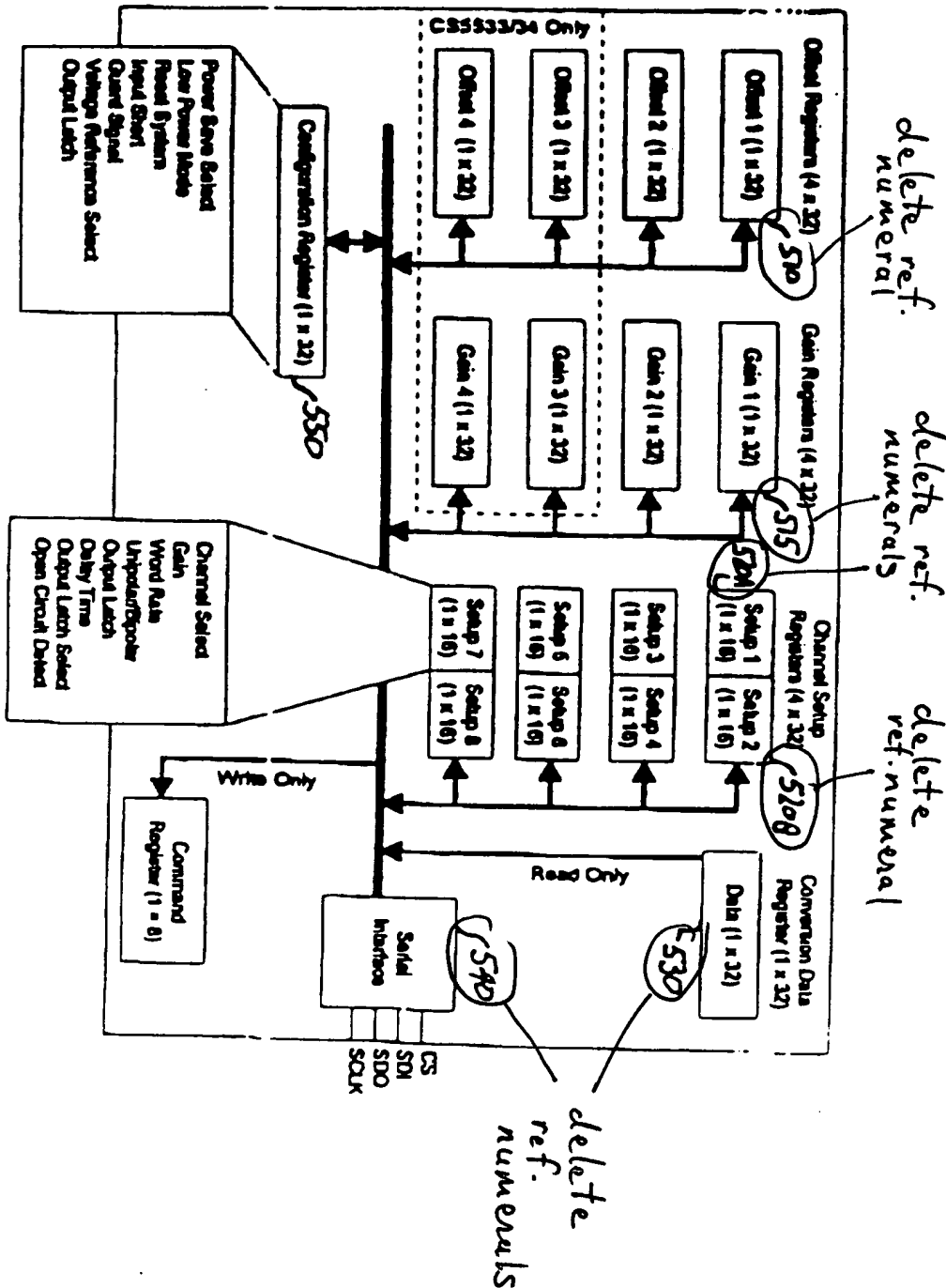


FIGURE 1.6A

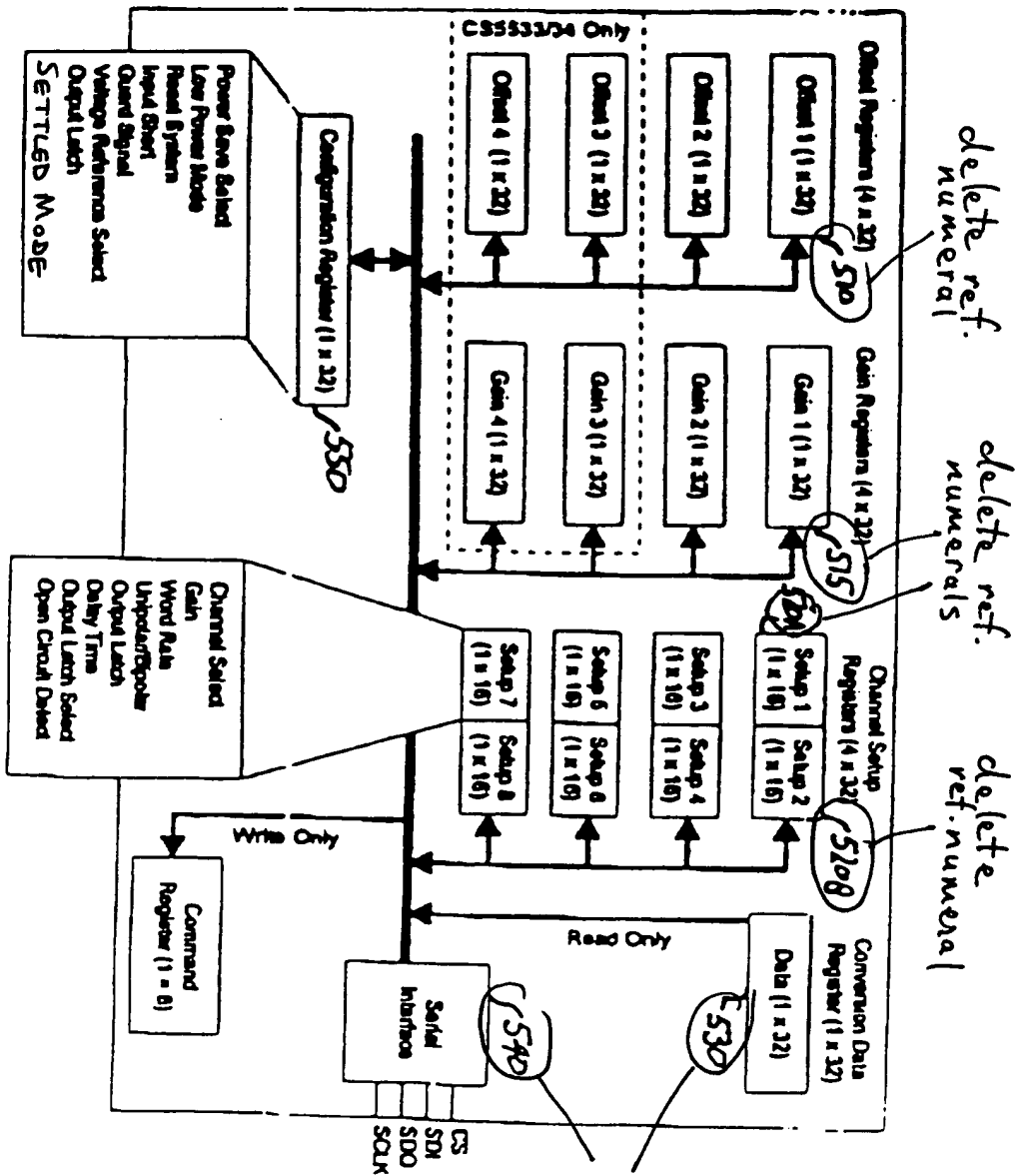


FIGURE 1.6B